IN THE SPECIFICATION:

Please replace paragraph [0031] of the Specification with the following paragraph, showing markings of all changes relative to the previous version of the paragraph:

[0031] Following this, as shown in FIG. 8, the invention then removes the third mask 700. Then, the exposed portions of the etch stop layer 500 are removed in a selective removal process that does not affect the underlying spacers 300 (using, for example, a wet or dry HF etching process). The etch stop layer 500 prevents the process of removing the second spacers 502 from affecting the first spacers 300. Note that the etch stop layer 500 will remain between the first spacers 300 and the second spacers 502 on the PFET structures 104. Finally, the oxide layer 106 overlying exposed areas of the substrate 100 and the gate conductors 102, 104 not covered by the first spacers 300 and the second spacers 502 are silicided to form silicide regions 800.

Please replace paragraph [0038] of the Specification with the following paragraph, showing markings of all changes relative to the previous version of the paragraph:

[0038] After this, as shown in item 920, the invention forms a third mask over regions of the substrate to be occupied by the PFETs. In item 922, the invention removes the second spacers from the NFETs, and then removes the third mask (924). Finally, the oxide layer overlying exposed areas of the substrate and the gate conductors not covered by the first spacers and the second spacers are silicided (926).